AMENDMENT TO THE SPECIFICATION

[0014] Reference is made to Figures 1 and 2. A multi-level solid state memory device 110 includes a stack of levels 112 of write-once memory. The stack is formed on a substrate 114. Each level 112 includes main memory and address logic. Details of an exemplary level 112 are disclosed in assignee's U.S. Serial No. 09/911,974 filed July 24, 2001 (now U.S. Patent No. 6,535,418) and incorporated herein by reference.